Design of power multi-channel data acquisition system

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Abstract: Data acquisition refers to the automatic acquisition of non-electric or electric signals from sensors and other devices to be tested and sent to the upper computer for analysis and processing, mainly for data acquisition, storage, processing and control. In modern industrial production, more and more sensor signals need to be collected and processed in real time at the same time. The main technical indicators of data acquisition module, such as sampling rate, resolution, input voltage range, control mode and anti-interference ability, are also increasingly demanded. A new data acquisition system that can realize multi-channel, multi-range signal acquisition and power supply will greatly facilitate signal acquisition and sensor field use. This paper presents a data acquisition system based on high-speed and multi-channel synchronous acquisition of power grid signals. MAX125 is the core of analog-to-digital converter and TMS320LF2407A is the core of data processing operate AD.

1. Introduction

With the development of China's industry, people's consumption of electric power is also increasing day by day. Nowadays, people put forward higher requirements for power system, not only to meet the requirements of continuous power supply, but also to pay more attention to power quality, especially the harmonic content of power grid and the instantaneous disturbance of voltage. In order to obtain the basic parameters of power grid operation, real-time data acquisition and operation must be carried out while it is running. A data acquisition system based on MAX125 and TMS320LF2407A is designed in this paper. The digital signal processor TSM320LF2407A has built-in 10-bit ADC with sampling and holding, but it can only receive 0-3.3V unipolar signals. For AC signals such as power grids, it needs to design boost limiting circuit. The crosstalk of each channel in the same sequencer is serious. For 5V signals, 5/2 = 0.00488, for 5V signals, it needs to design boost limiting circuit separately. For power system signal acquisition, AD converter with DSP is difficult to meet the error requirement within 0.05% of the design target, so AD bits should be at least 12 or more. Usually, AD converter bits should be at least one bit higher than the minimum resolution required. Therefore, we abandon the built-in AD converter with DSP and adopt at least 12-bit ADC external pieces[1].

2. Working Principle of the System

Data acquisition and monitoring system includes upper computer and lower computer system. The lower computer is composed of ARM industrial control development platform, data acquisition board, analog output board, LCD LCD display screen and SD memory card. The task is scheduled and managed by using the real-time multi-task operating system of UC/OS II. The multi-channel acquisition function of the data acquisition board for external analog data is realized, and the data is stored in SD card through USB. Or Ethernet transmission to the upper computer; under the control of the upper computer, the lower computer receives analog output instructions to complete the analog output function; LCD LCD screen is used to display the working status information of the lower computer. The upper computer communicates with the lower computer through USB or ethernet, receives the data collected by the lower computer and monitors it in real time. It graphically displays the curve of data change, and can set up the output of analog quantity, so as to

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control the output of analog quantity of the lower computer[2].

3. Design and Implementation of System Hardware

MAX125 is a 14-bit DAS (Data-Acquisition System) with a high-speed, multi-channel built-in synchronous sampling and holding circuit. It contains a 14-bit successive approximation ADC with a conversion time of 3 s, an internal 2.5V reference voltage and a slow reference input. Impulse, 4 high-speed sample-and-hold circuits, each sample-and-hold circuit corresponds to two input signals, so up to 8 signals can be converted. MAX125 uses bipolar power supply with input voltage range of + 5V and supply voltage of + 5V. High-speed parallel interface and bus timing characteristics can be connected with most MCUs or DSPs.

At the rising edge of each pulse, the on-chip sample-and-hold amplifier maintains the voltage and initiates an AD conversion. By default, only group A 1 channel can be converted, and MAX125 can be programmed by four bidirectional data/address lines, D0/A0-D3/A3, so that MAX125 can work in at least one channel, with a maximum of four channels plus a total of nine modes of power saving. Once programmed, this mode of work will be maintained continuously unless it is programmed again.

When MXA125 is converted according to the set working mode, the pin will generate interruption signal after the last conversion, triggering interruption at the descending edge. The signal will always become effective after the last conversion, and temporarily save the conversion results in the internal 14*4 RAM, control words (A0-A3) and output data (D4-D). 13) Input and output operations are performed through a three-state interface. When the conversion is completed, four consecutive reading pulses are applied to the pins to read the conversion results. It should be noted here that the data can not be read at will, but can only be read according to the number of conversion channels in the set working mode. That is to say, the first RD pulse can only be one channel of group A or group B. It takes several reading pulses to convert several channels.

How to access two MAX125 in parallel and how to control the sampling process is one of the key links in this design. For the TSM320LF2407A selected in this design, the 64K I/O space unique to DSP provides convenience for the expansion of external devices. In order to facilitate the reading and writing of MAX125 by DSP in software program design, this design takes two pieces of MAX125 as external devices of DSP and operates them through I/O mode. That is to say, two pieces of AD are set as I/O port address variables, through which the purpose of operation can be easily achieved. Here, if only one piece of MAX125 can be connected to the chip selector of AD through the external I/O space gated pin of the DSP, however, for the two pieces of MAX125 designed in this paper, in order to occupy the I/O address outside the DSP, a decoder is selected here to realize the function of address decoding to complete the chip selection of the two pieces of AD by the DSP. Using FairChild's 74HCT 139.

74HCT139 is a high-speed 2-4-line decoder with two independent input and output ports. In this way, two MAX125 chip selectors are connected to the two output ports of the decoder separately, which can solve the problem of chip selection of two MAX125 chips by DSP. Because MAX125 is a 14-bit A D, for convenience, the highest address lines A14 and A15 of the DSP are connected to the A0 and A1 terminals of the decoder, and the chip selectors connecting the first MAX125 chip are output and connected. At the other end, when the first MAX125 is selected, the end output is low, and the address of the MAX125 occupying the external I/O space of the DSP is 0000H; when the second piece is selected, the end output low level, which occupies the 4000H of DPSI/O space. Through the address decoder, the operation of MAX125 becomes much more convenient. It is realized that the two addresses are set as I/O port variables unique to DSP, and the specific address operations are replaced by variables. Obviously, the operation of variables is simple and efficient in programming[3].

In addition, because MAX125 is 5V working voltage and DSP is 3.3V, level conversion circuit is needed. In this paper, Phillips (PHILIPS) 74HC425 8-bit bus transceiver is used as level conversion device. 74HC245 can make the output voltage at Vcc level according to the setting of supply voltage Vcc: Simply speaking, output = Vcc, its biggest characteristic is that all input pin

voltage can be higher than Vcc, which is very useful for this design. Here, the Vcc = 3.3V power supply is used. The 5V of MAX125 can be added to the input without damaging the pins. The output 3.3V can be directly connected with the DSP, in which the output enabler and the DIR are directional control[4].

Three-phase voltage signals U, U and U enter from CH1A, CH2A and CH3A of the first MAX125 and three-phase current signals I, I and I enter MAX125 of the second MAX125. It should be noted here that the start signal of MAX125 is started by pulse and does not need chip selection. That is to say, as long as the level is low, AD will start to convert, and the output frequency doubling of PLL is the start signal. So once the PLL output is stable, MAX125 will start to convert, and the DSP can not control, let alone read. So the design uses the AND gate, one input is the PLL frequency doubling signal, the other is the digital I/O port (IOPE2) of the DSP. The low level output of IOPE2 indicates the start of AD conversion, so that DPS can control when MAX125 starts sampling. In normal operation, MAX125's working mode is set by lowering and lowering the address decoder and writing the control word to the bi-directional address data multiplexing pin. Each chip chooses the first three channels of group A as input. When the PLL is stable, the output control signal of DSP starts to start AD. When the three channels are converted in turn, the signal is generated. Here, or The gate ensures that two pieces of MAX125 are converted at the same time before they are valid. The interrupt signal is connected to the external interrupt X1INT of the DSP. The DSP determines whether the external interrupt occurs or not by means of detection. After confirming the interrupt, the conversion results are read in the external interrupt service program and stored in its memory. Some of the procedures are listed as follows:

```
ioport unsigned int port0000；  // Define the first MAX125 as the I/O port variable port0000
ioport unsigned int port4000；  // Define the second MAX125 as the I/O port variable port4000
#define MAX_125_fir port0000
#define MAX_125_sec port4000
MAX_125_fir=2；  // Write two pieces of MAX125 working mode to make it work in group A 3 channels
MAX_125_sec=2；
void AD_xint1()
{ AD_result_Ua[m]=MAX_125_fir；// Continuous reading of the results of the first three transformations
AD_result_Ub[j]=MAX_125_fir；
AD_result_Uc[k]=MAX_125_fir
*XNT1R = *XINT1R|0x8000；// Clear interruption mark
asm(" CLRC INTM")；  // Open total interrupt }[5]
```

4. Software design

4.1. Software Design of Lower Computer

The lower computer adopts the real-time multi-task operating system of Mu C/OS II. Mu C/OS II is a real-time multi-task operating system with open source code, portability, solidification, tailorability and preemption. It manages tasks based on priority completely, and always makes the tasks with the highest priority in the ready state run. Time slice rotation scheduling is not supported, so the system function must be reasonably decomposed into several tasks with different priorities according to the importance and real-time requirements. The rationality of task and priority Division will directly affect the quality of software design.

When dividing system functions into tasks, we should first make all tasks meet the real-time requirements, even in the worst case, all functions that require real-time in the system can be realized normally, and the number of tasks should be reasonable, and the software system should be simplified to reduce the demand for resources. According to the working principle and task division principle of data acquisition and monitoring system, the tasks of the lower computer system are

divided into USB communication task, Ethernet communication task, SD card writing data file task, data acquisition task, LCD display task and analog output task. In addition, the task of urgency and speediness is given higher priority, and the task of human-machine interface display is given lower priority because of low real-time requirement. The priority division is shown below.

①TASK1 task, priority 1, USB communication task;

②TASK2 Task, Priority 2, Ethernet Communication Task;

③TASK3 Task, Priority 3, SD Card Write Data File Task;

④TASK4 Task, Priority 4, Data Acquisition Task;

⑤TASK5 Task, Priority 5, Analog Output Task;

⑥TASK6 task, priority 6, LCD LCD display task.

In the software system of the lower computer, the communication between tasks is mainly accomplished by message mailbox. Message mailbox is used to pass a pointer between tasks or between interrupts and tasks so that tasks can send and receive any type of data through the pointer. Three message mailboxes are defined. Message mailbox 1 is used for data acquisition task to transmit data to communication task; Message mailbox 2 is used for communication between communication receiving task and analog output task; Message mailbox 3 is used for data acquisition task to send data to SD card to write data file task. As shown in the following program statement, the message mailbox pointer must be defined first, then the message mailbox is created, and finally waiting for other tasks to send mailbox or mailbox to other tasks.

```
OS EVEN T  * mbox ;// Define message mailbox pointer
mb ox =OSMboxCreat e(NULL);// Create a message mailbox
OSMb ox Pend(mbox , 0 , &err);// Waiting for message mailbox data
OSMb ox Pos t(mb ox , Buf);// Send message mailbox with data in buffer Buf
```

When the application runs, it first calls OSInit () to initialize C / OS II, then creates tasks by calling OSTa skCreate () in turn, and then executes OSStart () to start the multi-task environment, so as to schedule multi-task management. In the data acquisition task, after the board initialization is completed, the acquisition function is started periodically by using timer. The data of each acquisition port is read by query mode, and the arithmetic average filtering process is carried out. The sampled values are read five times continuously for arithmetic average operation. Then the data is transmitted to communication task and SD card through message mailbox. Write data file tasks.

Using ADS1.2 to develop the lower computer application program, using LPC2400 series special engineering template, because Smart 2400 development board is embedded with the operating system of C/OS II, it is not necessary to transplant the operating system during the development process, just load the source file of C/OS II into the project, and use the source file, driver file and header of the program. Files are modified and loaded accordingly. After compiling and linking is successful, they can be burned and written to Flash through the simulator[6].

4.2. Software Design of Upper Computer

PC data acquisition and monitoring software is developed using VC + + 6.0. When both USB and Ethernet are connected, USB is used to communicate. The main functions are as follows: 1) communicating with the lower computer through USB and Ethernet; 2) creating data receiving threads, receiving data collected by the lower computer through the communication interface, displaying the data on the monitoring interface in real time, and drawing data change curve; 3) setting the corresponding analog output value through the upper computer software to control the lower computer. The computer performs analog output work; 4) Display the connection status of communication interface and the working status information of the lower computer[7].

5. Experimental verification

In order to verify the data acquisition and monitoring system, the four output channels of analog output board are connected with the acquisition channels 1, 2, 3 and 4 of the data acquisition board respectively. The analog output board is controlled by upper computer software to output analog

voltage with an initial value of 1.5V. After a period of delay, the output voltage decreases linearly to 1.0V, and finally remains at 1.0V. The delay time is set to 100s by data acquisition and monitoring software. The IP address of the lower computer is 192.168.1.2, and the IP address of the upper computer is 192.168.1.3, so that both of them are located in the same LAN. After the "Setup" button of the upper computer software is pressed, the analog output board of the lower computer starts to output four channels of analog voltage. The output value decreases linearly from 1.5V to 1.0V after 100s. The data acquisition board collects the analog voltage and transmits the data to the upper computer and stores it to the SD card. The upper computer software monitors the collected data in real time and draws the data change curve. Through the experimental verification, the system has successfully realized the function of data acquisition and monitoring, completed the data acquisition, monitoring, storage and output of analog quantities. The system has good real-time performance and stability in the process of operation[8].

6. Conclusion

Based on MAX125 ADC chip, this paper designs a high-speed multi-channel data acquisition system for power network. Through address decoding and level conversion, it ingeniously solves the reading and writing operation of DSP, which has a certain practical value.

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